R22

Code No: 183AH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, December – 2024/January -2025
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, CE(SE), CSE(CS), CSE(DS), CSD)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of **ten questions** (numbered from 2 to 11) **carrying 10 marks each**. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A

(10 Marks)

1.a)	What is Mainframe Computer?	[1]
b)	Compare computer organization and computer architecture.	[1]
c)	What is the difference between a microprocessor and micro program?	[1]
d)	What is a control memory?	[1]
e)	Define partial remainder.	[1]
f)	What do you mean by 2's complement?	[1]
g)	What is the use of cache memory in computers?	[1]
h)	Differentiate between RAM and ROM.	[1]
i)	Write about delayed branch.	[1]
j)	Define operand forwarding.	[1]

PART-B

(50 Marks)

2.a)	Discuss the effect of clock frequency on the speed of operation of computers.	
b)	List the registers for the basic computer and give their functionality in program execution.	[5+5]
	OR	
3.	Describe various phases of instruction cycle with its flow chart.	[10]
4.	Explain how control signals are generated using micro programmed control.	[10]
	OR	
5.	Define an addressing mode. Explain about various addressing modes.	[10]
6.	Multiply $(-7)_{10}$ with $(3)_{10}$ by using Booth's multiplication. Give the flow table of the multiplication.	[10]
	OR	
7.	Draw and explain adding and subtracting numbers in signed 2's complement representation.	[10]

8. Discuss the different mapping techniques used in cache memories and their relative merits and demerits. [10]

OR

9.a) List and explain the merits and demerits of isolated I/O and memory-mapped I/0.
b) Give a neat sketch that illustrates the components in a typical memory hierarchy. [5+5]

10. Does pipelining get affected by data dependencies among the instruction? Justify your answer with lucid examples. [10]

OR

11.a) Explain the implementation of instruction pipelining in detail.
b) What is cache coherence problem? Discuss about different cache coherence approaches. [5+5]

---ooOoo---